File No Prn.SA/J/9/2021-PROJ
GOVERNMENT OF INDIA
CABINET SECRETARIAT
OFFICE OF THE PRINCIPAL SCIENTIFIC ADVISER
TO THE GOVERNMENT OF INDIA

VIGYAN BHAWAN ANNEXE
MAULANA AZAD ROAD
NEW DELHI - 110 011
Phone: +91 11 23734553
FAX: +91 11 23022116

Sub: Minutes of the 1st Stakeholder Meeting to discuss the proposal of Indian Institute of Science Bangalore on the establishment of a 2D Material Based Future Semiconductor Technology Centre / Innovation Hub

The subject meeting was held on the 21st January 2022 over video conferencing. This was the first meeting in a series of stakeholders' meetings and deliberations required for developing a DPR on said subject. Earlier, IISc was asked by the PSA's office (***Annexure-I***) on the recommendation of the PSA and Dr Saraswat (NITI Aayog) to submit a DPR on their said proposal (***Annexure-II***). Over 180 eminent members from various leading academic institutes of India, Industry experts and invitees from the Office of the Principal Scientific Adviser to the Government of India (PSA's Office), Ministry of Electronics and Information Technology (MeitY), Department of Science and Technology (DST), Department of Space (DoS), Department of Atomic Energy (DAE) and Defence Research and Development Organisation (DRDO) attended the meeting. A complete list of participants is annexed (***Annexure-III***).

2. The meeting started with welcome remarks from Prof. Mayank Shrivastava, Indian Institute of Science (IISc) Bangalore. He gave a brief overview of the initiative and the steps undertaken thus far. He requested inputs from the academic peers and the members from strategic sector / Govt. ministries to make this a successful and sustainable endeavour, on the detailed presentation that was to follow.

3. Dr Preeti Banzal, Adviser and Scientist 'G', PSA's Office welcomed this timely initiative from IISc, Bangalore, and assured all support from the PSA's Office.

4. Prof. V. Ramgopal Rao, Director, Indian Institute of Technology (IIT), Delhi commented that this is a great initiative covering a very broad area. Hence, it requires a technology development innovation hub/centre which also leads to a consortium of leading experts and stakeholders. He suggested using learning from the NNetTRA and INUP programs of MeitY for the proposed 2D CoE in such a way while a technology-focused

centre is established to meet the roadmap set by the industry, it would also be beneficial for the academic/scientific community in India.

5. Dr Harald Gossner, Sr. Principal Engineer, Intel, strongly recommended such a centre from the semiconductor industry perspective. He also gave an insight on the technology initiatives at Intel, and the global perspective of 2D materials as the next big technology beyond Silicon. He recommended that it is imperative for India to invest now in this technology to be future-ready.

6. Prof. Mayank then gave a detailed presentation, based on the brief proposal that was circulated earlier. After the presentation, inputs were invited from all the participants. Unanimous support and appreciation were received from all sectors including experts from academia. A detailed transcript of the deliberations that took place, inputs given, and comments made are attached (***Annexure-IV***).

7. Following is a summary of the major clarification given by Prof. Mayank on the questions/observations raised and suggestions offered by the participants:-

a. The proposed CoE /Hub will not be an academic department /centre of IISc. It will eventually be a Section 8 company in terms of operation (or a similar model to ensure the centre of excellence or innovation hub), situated inside the IISc campus or inside IISc's research park / existing innovation park.

b. The focus of the proposed innovation centre/hub is on 2D Semiconductors such as Transition Metal Dichalcogenides, i.e., technologies that leading semiconductor industries (such as Intel, TSMC, etc.) are pushing and technologies which are in IRDS and Quantum roadmap. The proposed effort is primarily on technology development & scale-up. The proposed technology roadmap also focuses on technology development & scale-up while catering to applications like electronics, sensing, neuromorphic, optoelectronics and quantum. Graphene will be included in the technology roadmap, only to integrate Graphene with 2D Semiconductors in complex device/process integrations or use Graphene for very specific technology development, particularly of interest to industry and strategic, for example, graphene-based THz detectors, EMI shield and heat spreaders, which have not been yet been taken up.

c. The proposed centre can be seen as equivalent to an early day's Bell Labs or a Semiconductor R&D Fab (say IMEC). Most of the developments will happen at the centre but the centre may outsource certain problems to be addressed, which require deeper investigations and research, to other academic groups. The problems outsourced will be a small fraction of the overall technology development effort that the centre would put in place and would be of low TRL

nature (TRL 1-3). However, the proposed centre's effort will be on high TRLs (TRL 4-8). The objective of the proposed centre is to develop Electronics, Sensing, Neuromorphic, Memory, Optoelectronics & Quantum technologies, using 2D material-based platforms, which has already become quite relevant to leading semiconductor industries like Intel, TSMC, etc. – as suggested by the industry roadmap.

d. From the outsourced problems, once a solution is developed, the IPs, knowhow, process, etc will be transferred to the centre under a certain pre-agreement for IP transfer. This will be the job of the 2D Research Consortium, which will be part of the proposed 2D Technology/Innovation Hub.
e. The centre would also cater to various needs of the academic/scientific community in India like availability of high-quality material, availability of devices to test/investigate/experiment, availability of PDK for circuit design, availability of process knowhow, access to industries, etc.
f. Experts from different academia will be able to engage with the CoE in a very similar way as anyone engages throughout the world with IMEC's centre (which is only at one place in the world). IMEC focuses on a range of technologies while this centre will work only on technologies based on 2D materials.
g. While the ongoing effort has already helped build synergy with various 2D experts in India and with those who would like to get into this area, in terms of operations, execution model and technical roadmap we are committed to building synergy with the extant govt. initiatives..
h. Semiconductor technology/product development involves the integration of complex processes, all developed using a dedicated tool line inside a highly controlled environment. The infrastructure must be at one location. While building the Fab line which may take initial 2 years, the centre will fund specific developments to 2D technology experts in India (experts across institutes, including IISc) through a competitive call.
i. Another objective of this centre will be to connect different experts in the 2D technology areas across the country and the Indian diaspora to build and demonstrate an international level of strength. The centre will also take advantage of expertise and technology know-how/IP available across the country.
j. The 2D CoE effort will also help with the fundamental aspirations of the 2D related scientific community in India if their efforts are going to be

technologically relevant a few years down the line. These are the low TRL threads that we will pursue from the beginning along with high TRL activities.

k. Some of the industries have promised to offer their high-end industry standard growth tools, growth recipe, and support personnel to deliver high-quality electronic grade material which they already have through their developments at other places like IMEC, Cambridge, 2D-EPL, etc. They have promised to transfer all this in return for learning how their material behaves when one runs the entire device/circuit process and what challenges/issues might require further material engineering. This will help co-designing material, device and process together with the goal of achieving desired performance with high yield and reliability. Further development from the unit process to end product would be done in-house by the COE, and the know-how generated will be available for the industry and other beneficiaries, through a suitable model.

l. The tool companies have offered only the process/recipe and experience to scale it up here locally. CoE will not be relying on imported materials or technologies, but only on a base recipe to get a head start. The quality of the material will be improved locally through feedback from the process. The process, devices, technology, designs, products, etc. will be developed locally at this centre.

9. The participants looked forward to this initiative and the centre.

10. The meeting ended with a vote of thanks at 1900 hrs.

*****

Annexure-I

(Refers Para 1 of the Minutes)

F. No. J/9/2021-PROJ .
Office of the Principal Scientific Adviser
to the Government of India.

328, Vigyan Bhawan Annexe,
Maulana Azad Road,
New Delhi-110011.

Dated: 29th October, 2021

To,

Prof. Govindan Rangarajan
Director
Indian Institute of Science, Bangalore

Subject: Request for deliberations to prepare a detailed project report (DPR) on a Centre of Excellence for 2D Material Based Future Technology research (2D Materials Innovation and Technology Centre)

Dear Sir,

I am writing to you regarding a proposal submitted by the IISc team, led by Prof. Mayank Shrivastava, to our office early this year. The proposal was to establish a Centre of Excellence (COE) for two-dimensional (2D) materials-based future technology research.

Given the immense potential of this emerging technology and how fast the world is moving at this front, the PSA office shared the proposal with Dr. V. K. Saraswat (Hon'ble Member, NITI Aayog), who also chairs the empowered committee for Semiconductor Fabs. A meeting with Dr. Saraswat, members from the S&T vertical of NITI Aayog, and the PSA's office was scheduled on September 23rd. The IISc team gave a detailed presentation on this proposal. The minutes of this meeting are enclosed as an attachment for your reference.

As a follow-up to the discussions held on September 23rd and inputs given to the IISc team, I am writing to you on behalf of this Office, to submit a detailed project report (DPR) on the proposed CoE. The deliberations required for the DPR are listed below:

Stage 1:

(a) Build a DPR drafting team consisting of experts from IISc Bangalore (lead institute), an industry expert, MeitY and PSA's office as primary Members.
(b) Organize meetings with stakeholders for laying out a roadmap. The deliberations required for the DPR will involve interactions with stakeholders from govt. (PSA Office, relevant ministries, etc.), strategic (ISRO, DRDO, etc.), academia in India and abroad, and potential industries having an interest to partner/collaborate in the future.
(c) Review and study such international centres (e.g., Manchester, Cambridge, IMEC, etc.) and their ongoing developments.
(d) Create a road map for the CoE along the lines of, if not better than, similar centers worldwide, with a focus on key technologies to be developed around a backbone.
(e) Align with industry for scale-up.
(f) Ascertain IP transfer needs for strategic players and commercial entities.

Stage 2:

(a) Layout the concept and design of proposed CoE including new infrastructure required and how existing infrastructure will be augmented.
(b) Derive a technology roadmap (Electronics, Sensors, Neuromorphic, Quantum, Optoelectronics, Photonics, THz, Packaging, etc.)
(c) Layout the governance structure, human resource availability in India and support required for its success.
(d) Model for financial sustenance beyond ten years.
(e) Detailed project timelines for five years and funding required for first five years.

Stage 3:

Submit the final version of the DPR to be evaluated by PSA and the Empowered Technology Group for FAB set up by MeitY.

The DPR must also account for the inputs summarized in the attached minutes of the meeting. Mr. Shirish Panda, from the PSA office, will assist the IISc team with the said deliberations and stakeholder meetings required. We request you to submit the DPR as early as possible, preferably within six weeks. We are looking forward to hearing from you and IISc team soon.

Attachment:
(1) Minutes of the meeting, held on September 23rd, 2021, chaired by Dr. V. K. Saraswat (Hon'ble Member, NITI Aayog)
(2) An initial draft of the 2D CoE proposal.

(Jitendra R Gaikwad)
Deputy Secretary (Admn)

Cc:

(1) Dr. V. K. Saraswat, Hon'ble Member, NITI Aayog
(2) Prof. K. Vijayraghavan, Principal Scientific Adviser to the Government of India,
(3) Prof. Mayank Shrivastava, Indian Institute of Science, Bangalore

Annexure-II

(Refers Para 1 of the Minutes)

Proposal to Establish a Centre of Excellence (CoE) & Consortium for Future Heterogeneous Technologies Using 2-Dimensional Materials

Indian Institute of Science, Bangalore (Contact*: Mayank Shrivastava, email: mayank@iisc.ac.in)

*IISc team consists of 30+ faculty members. The consortium would consist of the IISc team, 25+ experts from the rest of the world, and 10+ industries, who have already signed up.

1. What? – Hunt for Future Nanoelectronic, Sensing, Optoelectronics, Neuromorphic & Quantum Technologies

The evolution of semiconductor technology, particularly Si technology, has been a critical driver for the technological advancements that we see around us. The Si industry has come a long way from using 2250 transistors in Intel's 4004 (1971) to 11.8 billion transistors in Apple's A14 Bionic microprocessor (2020). A lot has changed over the years, not just in terms of the number of transistors per unit area & frequency of operation, but also in terms of desired functionalities and applications given the nature of products that demand heterogeneous capabilities. Going further, conventional bulk semiconductor technologies find it challenging to meet future technology requirements. Therefore, the end of Moore's law and the emergence of beyond-Si electronics, optoelectronics, and quantum technologies are well-accepted directions of the last decade. Heterogeneous integration of various functionalities, including sensing, neuromorphic, Optoelectronics, and Quantum technologies, is projected to be the driving force for industries in the coming decades. The projected future requirements demand technologies such as flexible & wearable electronics, bio-implantable & flexible neuromorphic processors, THz electronics, multi-dimensional sensors and sensory systems, and quantum-enhanced systems for computation, sensing, and communication. This has pushed stakeholders to think of universal technology platforms and better ways to meet future applications' needs. Among various emerging materials, 2-Dimensional (2D) materials like graphene and TMDCs promise to offer solutions to existing issues/bottlenecks with conventional bulk platforms. Besides, they open opportunities for a plethora of new/disruptive applications and, henceforth, possibilities of new markets. Keeping in mind the promises of 2D materials and various applications it can cater to, a 2D material-based universal technology platform for heterogeneous integration is inevitable. These are the reasons why the world has moved too fast on 2D materials research and leading industries like Intel, TSMC, and industrial R&D centers like IMEC have made significant investments on this technology. On the other hand, efforts in India are relatively small.

2. Why? – Industry Roadmap for Heterogeneously Integrated Nanoelectronic & Quantum Enhanced Technologies

Worldwide efforts using 2D materials though cover the entire spectrum from beyond-Si electronics to quantum technologies (See Fig. 1, the Year 2004 – 2015); the approach followed until recently has been disconnected. From an industrial perspective, a universal platform would be the most efficient and cost-effective way to enable heterogeneous integration. Keeping this in mind, the industry has started focusing on this direction (See Fig. 1, the Year 2017 – 2020). Fig. 2 depicts a projected heterogeneously integrated system, expected to be enabled by a universal 2D material technology platform. This would require dedicated science and engineering efforts to enable a universal technology platform catering to a range of 2D materials-based products and heterogeneous integration, as projected in Fig. 1 (The year 2020 – 2030).

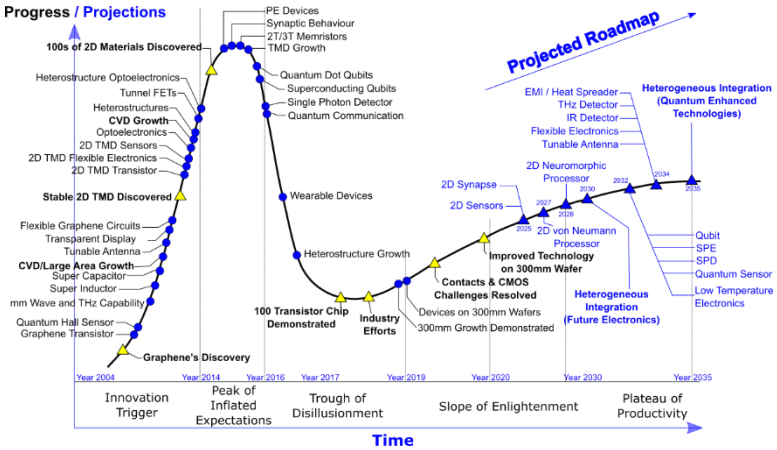

Figure 1: A projected roadmap for 2D materials and 2D material-based technology enablement.

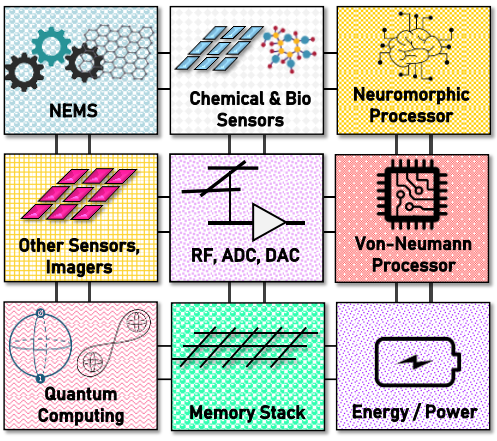

Figure 2: Projected possibility and ability of 2D material-based universal technology platform to enable heterogeneous integration of future electronics, optoelectronics, and quantum enhanced technologies.

Keeping in mind that India can encash 2D materials-based technologies, efforts in India need to be scaled up. Therefore, we envision and propose efforts like existing international 2D/graphene centers (in USA/UK/EU) in a consortium mode, however, with a focused effort on enabling technology platforms that would cater to a range of future products based on 2D materials. These products, IPs, know-how developed, and research conducted would place India at the forefront of 2D

material-based nanoelectronic, sensing, optoelectronics, neuromorphic, and quantum technologies. Besides, it should generate enough traction to encourage industries to establish technology development efforts in India.

3. How? - Consortium Details, Funding Required, Engagement, Operational & Revenue/Sustenance Model

We envision efforts like existing international 2D/graphene centers (in USA/UK/EU) in a consortium model (Fig. 3) through a Centre of Excellence (CoE) proposed to be established in IISc. This CoE will have a charter to (i) build capacity and technology knowhow, (ii) work with leading experts and industries in a consortium mode, (iii) develop technology platforms for 2D material based products, which would also cater to R&D on various 2D material threads and needs of different groups/industries around the world, (iv) demonstrate a few 2D material-based products – as a technology demonstrator – involving heterogeneous integration, (v) use the universal technology platform to enable other/quantum applications and (vi) strengthen and expand 2D material-based technology development efforts in India to put India at the forefront of 2D materials-based nanoelectronic, sensing, optoelectronics, neuromorphic, and quantum technology research/development.

The consortium will consist of experts from IISc and several other leading institutes worldwide. Besides, we also envision vibrant industry participation. The IISc team consists of 30 faculty members with expertise ranging from 2D materials growth, device physics/processing, and modeling and circuit/system design. This expertise has been complemented by faculties from top institutes in India (various IITs), the USA (UCSB, Rice, Penn State, UT Austin, Vanderbilt, UC Florida, and UCLA), and UK (Cambridge and Manchester). We have received expressions of interest to join the consortium from 23 leading graphene/2D experts worldwide. Various modes in which these experts can engage within the consortium have also been worked out. Similarly, the team has also reached out to 18 leading/global industries that may have an interest or ongoing development in Graphene or 2D materials-based applications. These are Intel, Texas Instruments, Samsung, Cadence, Applied Materials, AIXTRON, OXFORD, etc. To begin with, we have invited such industries to sign-up for the proposed consortium by expressing interest in Graphene and 2D material-based technologies, technology development, or its products. In the future, when the center is established, we envision that such industries being part of the consortium will be engaging with the center directly under various modes bringing revenue, facilities, or knowhow. Besides, we have also triggered dialogues with already established graphene/2D centers (Cambridge, Manchester, NUS, and IMEC) to learn from their experiences and seek cooperation. Among these, Cambridge and Manchester have already expressed interest in partnering with India graphene/2D center. Finally, it is also envisioned that the consortium will be guided by an International Advisory Board, which will comprise top academicians and key players from leading semiconductor industries (Fig. 3).

This effort would require an initial investment of the order of 500 Cr. from the govt. However, after this initial investment, we envision self-sustaining the activities (beyond 5 years) through this center's services and technology licensing, and eventually achieving break-even in less than 10 years. These products, IPs, know-how developed, and research conducted would also place India at the forefront of 2D material-based nanoelectronic, sensing, optoelectronics, neuromorphic, and quantum technologies. Besides, we expect this effort to generate enough traction for leading industries to invest in 2D material-based technology efforts in India along the lines of investments IMEC attracts (Fig. 4).

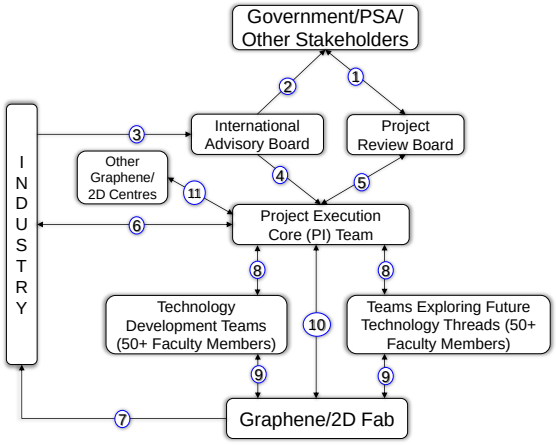

Figure 3: Consortium Structure & Operational Model of the CoE.

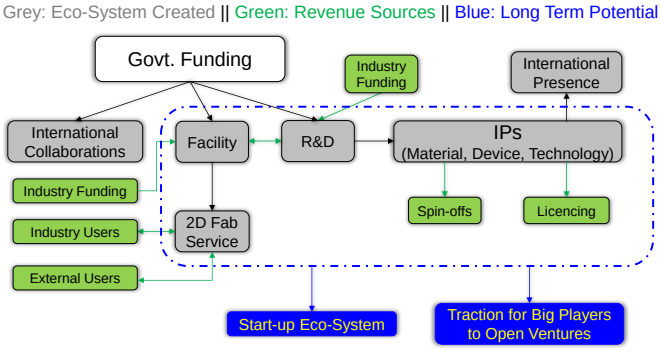

Figure 4: Eco-system expected to be created by this effort (Grey). Expected tangible outcomes of the CoE and revenue sources (Green). Long term growth potential (Blue).

Annexure-III

(Refers Para 1 of the Minutes)

List of Participants

1st Stakeholder Meeting to discuss the proposal of Indian Institute of Science Bangalore on the establishment of a 2D Material Based Future Semiconductor Technology Centre / Innovation Hub

Sl No	Name	Organisation
1	Dr. Preeti Banzal	PSA's Office
2	Prof. V. Ramgopal Rao	IIT Delhi
3	Dr. Harald Gossner	Intel, Germany
4	Dr. Sudesh Kumar Vasudeva	PSA's Office
5	Mr. Shirish Panda	PSA's Office
6	Mr. Sudhir Kumar Marwaha	MeitY
7	Dr. Sunita Verma	MeitY
8	Dr. Sandip Chatterjee	MeitY
9	Dr. Arvind Kumar	MeitY
10	Dr. Sangeeta Semwal	MeitY
11	Dr. Murali Mohan	DST
12	Dr. Swati Rawal Dang	DST
13	Dr. Kalaivani Ganesan	DBT
14	Dr. Sona Das	SCL
15	Dr. Anil Raj Singh	DRDO
16	Dr. V. K. Aswal	BARC, DAE
17	Prof. Tarun Sharma	RRCAT, DAE
18	Dr. Sandip Dhara	IGCAR, DAE
19	Mr. Selva Kumar M	DYSL-CT, DRDO

Sl No	Name	Organisation
20	Mr. Akash Bain	DYSL-QT, DRDO
21	Dr. Sarala V.	RCI, DRDO
22	Mr. Manu Gaurav	LRDE, DRDO
23	Mr. Ravindra Prasad	LRDE, DRDO
24	Dr. Sudhir Khare	IRDE, DRDO
25	Prof. B Gurumoorthy	CEO, SID
26	Mr. Krishna Kumar Thirumalai Kuravai	SID
27	Prof. Anshuman Kumar	IIT Bombay
28	Prof. Kasturi Saha	IIT Bombay
29	Prof. Parinda Vasa	IIT Bombay
30	Prof. S Kotha	IIT Bombay
31	Prof. M. Aslam	IIT Bombay
32	Prof. Saurabh Lodha	IIT Bombay
33	Prof. Dipanshu Bansal	IIT Bombay
34	Prof. Aftab Alam	IIT Bombay
35	Prof. Shobha Shukla	IIT Bombay
36	Prof. Dipti Gupta	IIT Bombay
37	Prof. Sumit Saxena	IIT Bombay
38	Prof. Tanushree Choudhury	IIT Bombay
39	Prof. Saroj Nayak	IIT BBS
40	Prof. Niharika Mohapatra	IIT BBS
41	Prof. Dr Kisor Kumar Sahu	IIT BBS
42	Prof. Ashish Kumar Mishra	IIT BHU
43	Prof. Dr AMRITANSHU PANDEY	IIT BHU
44	Prof. Marshal	IIT BHU
45	Prof. Shivam Verma	IIT BHU

Sl No	Name	Organisation
46	Prof. Rajendra Singh	IIT Delhi
47	Prof. Samresh Das	IIT Delhi
48	Prof. P K Muduli	IIT Delhi
49	Prof. Krishna Balasubramanian	IIT Delhi
50	Prof. Dhiman Mallick	IIT Delhi
51	Prof. Madhusudan Singh	IIT Delhi
52	Prof. Santanu Ghosh	IIT Delhi
53	Prof. Dibyajyoti Ghosh	IIT Delhi
54	Prof. Santanu Ghosh	IIT Delhi
55	Prof. Ankur Goswami	IIT Delhi
56	Prof. Naveen Kadayinti	IIT Dharwad
57	Prof. Ruma Ghosh	IIT Dharwad
58	Prof. Saroj Mondal	IIT Dharwad
59	Prof. Gagan Kumar	IIT Guwahati
60	Prof. Debabrata Sikdar	IIT Guwahati
61	Prof. Roy paily Palathinkal	IIT Guwahati
62	Prof. Saurabh Basu	IIT Guwahati
63	Prof. Girish Setlur	IIT Guwahati
64	Prof. Ravindra Kumar Jha	IIT Guwahati
65	Prof. Uday Narayan Maiti	IIT Guwahati
66	Prof. PAMU DOBBIDI	IIT Guwahati
67	Prof. Dr. Gaurav Trivedi	IIT Guwahati
68	Prof. Arun Tej Mallajosyula	IIT Guwahati
69	Prof. Nihar Ranjan Mohapatra	IIT Gandhinagar
70	Prof. DHIRAJ BHATIA	IIT Gandhinagar
71	Prof. Kabeer Jasuja	IIT Gandhinagar

Sl No	Name	Organisation
72	Prof. Karthik Subramaniam Pushpavanam	IIT Gandhinagar
73	Prof. Tarun Kumar Agarwal	IIT Gandhinagar
74	Prof. Shaikh M. Mobin	IIT Indore
75	Prof. Ajay Kumar Kushwaha	IIT Indore
76	Prof. Mukesh Kumar	IIT Indore
77	Prof. Rajesh Kumar	IIT Indore
78	Prof. Shaibal Mukherjee	IIT Indore
79	Prof. Krushna R Mavani	IIT Indore
80	Prof. Peayush Kumar Choubey	IIT ISM Dhanbad
81	Prof. MANODIPAN SAHOO	IIT ISM Dhanbad
82	Prof. Lutukurthi D N V V Konda	IIT ISM Dhanbad
83	Prof. Jitendra Kumar	IIT ISM Dhanbad
84	Prof. Amitava Adak	IIT ISM Dhanbad
85	Prof. MANOJ CHOUDHARY	IIT Jodhpur
86	Prof. Ajay Agarwal	IIT Jodhpur
87	Prof. Suresh Devasahayam	IIT Jammu
88	Prof. BISWANATH CHAKRABORTY	IIT Jammu
89	Prof. Yogesh Chauhan	IIT Kanpur
90	Prof. Shikhar Misra	IIT Kanpur
91	Prof. Somnath Bhowmick	IIT Kanpur
92	Prof. Basudev Lahiri	IIT Kgp
93	Prof. Tarun Kanti Bhattacharyya	IIT Kgp
94	Prof. Sankha Mukherjee	IIT Kgp
95	Prof. Sivarama Krishnan	IIT Madras
96	Prof. Shivananju Bannur Nanjunda	IIT Madras

Sl No	Name	Organisation
97	Prof. Pramoda Kumar Nayak	IIT Madras
98	Prof. Somnath C Roy	IIT Madras
99	Prof. Abhishek Misra	IIT Madras
100	Prof. Manu Jaiswal	IIT Madras
101	Dr. K. Lakshmi Ganapathi	IIT Madras
102	Prof. Ajay Soni	IIT Mandi
103	Prof. Viswanath Balakrishnan	IIT Mandi
104	Prof. Suman Kalyan Pal	IIT Mandi
105	Prof. Jayakumar Balakrishnan	IIT PKD
106	Prof. Soham Manni	IIT PKD
107	Prof. Arvind Ajoy	IIT PKD
108	Prof. Revathy Padmanabhan	IIT PKD
109	Prof. NAGENDRA PRASAD PATHAK	IIT Roorkee
110	Prof. Vimal Chandra Srivastava	IIT Roorkee
111	Prof. Gaurav Manik	IIT Roorkee
112	Prof. Vivek Kumar Malik	IIT Roorkee
113	Prof. Anirban Mitra	IIT Roorkee
114	Prof. Soumitra Satapathi	IIT Roorkee
115	Prof. Brajesh rawat	IIT Ropar
116	Prof. Devarshi Mrinal Das	IIT Ropar
117	Prof. Devarshi Mrinal Das	IIT Ropar
118	Prof. T. J. DHILIP KUMAR	IIT Ropar
119	Prof. Mukesh Kumar	IIT Ropar
120	Prof. Rajesh V Nair	IIT Ropar
121	Prof. Rohit Sharma	IIT Ropar
122	Prof. Rajeev Ahuja	IIT Ropar

Sl No	Name	Organisation
123	Prof. Khushboo Rakha	IIT Ropar
124	Prof. Neha Sardana	IIT Ropar
125	Prof. S S Padhee	IIT Ropar
126	Prof. Swapnil Bhuktare	IIT Tirupati
127	Prof. Kaushik Ghosh	INST Mohali
128	Prof. Kamalakannan Kailasam	INST Mohali
129	Prof. Jitendra Singh	CEERI
130	Prof. SANTANU KUMAR PAL	IISER Mohali
131	Prof. Chaitanya A Athale	IISER Pune
132	Prof. Ramanathan Vaidhyanathan	IISER Pune
133	Prof. Surjeet Singh	IISER Pune
134	Prof. Atikur Rahman	IISER Pune
135	Prof. Ashish Arora	IISER Pune
136	Prof. Mukul Kabir	IISER Pune
137	Prof. Vinayak B Kamble	IISER TVM
138	Prof. Rajendra Kurapati	IISER TVM
139	Prof. Bikas Chandra Das	IISER TVM
140	Prof. Sukhendu Mandal	IISER TVM
141	Prof. Rajeev N Kini	IISER TVM
142	Prof. Manoj A G Namboothiry	IISER TVM
143	Prof. Seena V	IIST
144	Prof. Shobhana Narasimhan	JNCSR
145	Prof. Kanishka Biswas	JNCSR
146	Prof. Atindra Nath Pal	SN Bose
147	Prof. H K Singh	NPL
148	Prof. Govind	NPL

Sl No	Name	Organisation
149	Prof. Bipin Gupta	NPL
150	Dr. B. B. Kale	C-MET
151	Dr. Raghu	C-MET
152	Dr. Seema	C-MET
153	Prof. Srinivasan Raghavan	IISc Bangalore
154	Prof. Navakanta Bhat	IISc Bangalore
155	Prof. Rudra Pratap	IISc Bangalore
156	Prof. Arindam Ghosh	IISc Bangalore
157	Prof. Akshay Naik	IISc Bangalore
158	Prof. Kausik Majumdar	IISc Bangalore
159	Prof. Sushobhan Awasthi	IISc Bangalore
160	Prof. Praveen Ramamurthy	IISc Bangalore
161	Prof. Sanjiv Sambandan	IISc Bangalore
162	Prof. Varun Raghunathan	IISc Bangalore
163	Prof. Baladitya Suri	IISc Bangalore
164	Prof. Abha Misra	IISc Bangalore
165	Prof. Chandni Usha	IISc Bangalore
166	Prof. Manish Jain	IISc Bangalore
167	Prof. Aveek Bid	IISc Bangalore
168	Prof. Anindya Das	IISc Bangalore
169	Prof. Abhishek Singh	IISc Bangalore
170	Prof. Navaneetha Krishnan Ravichandran	IISc Bangalore
171	Prof. Hardik Pandya	IISc Bangalore
172	Prof. Chetan S. Thakur	IISc Bangalore
173	Prof. K. J. Vinoy	IISc Bangalore

Sl No	Name	Organisation
174	Prof. Arup Polley	IISc Bangalore
175	Prof. Digbijoy Nath	IISc Bangalore
176	Prof. Shankar K. Selvraja	IISc Bangalore
177	Prof. Surya Sarathi Bose	IISc Bangalore
178	Prof. Prosenjit Sen	IISc Bangalore
179	Prof. Sourabh Chandorkar	IISc Bangalore
180	Prof. Santanu Mahapatra	IISc Bangalore
181	Prof. Utsav Banerjee	IISc Bangalore
182	Prof. Mayank Shrivastava	IISc Bangalore

*****

Annexure-IV

(Refers Para 6 of the Minutes)

Meeting Transcript

1st Stakeholder Meeting to discuss the proposal of Indian Institute of Science Bangalore on the establishment of a 2D Material Based Future Semiconductor Technology Centre / Innovation Hub

---

Proposal on a 2D Material Based Future Semiconductor Technology Center / Innovation Hub

PI: Prof. Mayank Shrivastava, Department of ESE, Indian Institute of Science

Lead Institute: Indian Institute of Science Bangalore

1st Stakeholder's Meeting: Friday, 21st January 2022; 4:00 – 7:00 PM

Attendees: Over 100 eminent members from various leading institutes in India, Industry Experts, and Invitees from PSA Office, MeitY, DST, DOS, DAE & DRDO (see detailed list at the end)

Meeting Started at 4:00 PM.

Prof. Mayank Shrivastava (IISc Bangalore) started with the overview of this meeting and the background of the overall initiative. He stated that this meeting is a Get-to-Know-more about the 2D Innovation Hub/Centre and welcomed inputs from the academic peers and members from strategic sector / govt. ministries to make this a successful and sustainable endeavour. Three years back when we envisioned a technology & innovation hub/center dedicated for 2D material-based semiconductor technologies, the idea was that while India missed the Si bus, we need to develop pathways to ensure we don't miss opportunities in future technologies. Therefore, rather than waiting to catch-up on future technologies, India must proactively invest in future (beyond Silicon) technologies by jumping the roadmap. An investment as proposed here will ensure that the country is ready for upcoming technologies beyond Silicon. In last 3 years, while we were discussing this proposal with various stakeholders, semiconductor industry and international community has made a significant progress on 2D materials based technology that now industry has integrated 2D technology on a 300mm platform. If we don't invest on this technology now, in a systematic and consolidated manner, with a focus on developing technologies of industrial interest, we may miss the 2D bus as well. Its high time that India takes pro-active measures. He further explained how PSA office proactively came forward and helped shape this proposal. Subsequently the proposal was sent to Dr. Saraswat of NITI Aayog who also chairs an empowered committee for semiconductor fabs and related things in India. The presentation given to a committee chaired by Dr. Saraswat with members from NITI Aayog and PSA's office received a whole-hearted support for this initiative. Subsequently the PSA's office requested IISc, through a letter dated Oct. 29th, 2021, to submit a detailed

project report. The letter also listed the deliberations required. This stakeholder's meeting is one such deliberation, to seek inputs from academic peers from various leading institutes. For this meeting PSA office requested all IIT/IISER/TIFR Directors (and Heads of C-MET, CEERI, NPL) to inform all their faculties about this facility. Everyone who works on 2D materials (both science and technology) or interested in this emerging technologically relevant field can contribute by giving their valuable inputs, and hence were requested to participate. Besides the team also wanted to take inputs from academic peers as to how this endeavour will be beneficial to the academic community, strengthen technology & financial roadmap and overall to make the initiative self-sustaining.

On behalf of PSA's office, Dr. Banzal added that this is a timely initiative. She assured all the help from the PSA office.

Prof. Ramgopal Rao (Director, IIT Delhi) commented that this is a great initiative as 2D is a very broad area consisting of different types of 2D materials, having a range of applications from nanoelectronics, sensing, memory, neuromorphic, optoelectronics, quantum, etc. Hence, it requires a technology development/innovation hub/center, which also leads a consortium of leading experts and stakeholders. India should have invested on this technology 10 years back like Europe did. Prof. Rao suggested to use learnings from the NNetRA and INUP programs of MeitY for the proposed 2D CoE in such a way that while a technology focused center is established to meet the roadmap set by industry, it would also be beneficial for the academic/scientific community in India.

Dr. Harald Gossner (Senior Principal Engineer, Intel) strongly recommended such a center from semiconductor industry point of view. Dr. Gossner is in Industry, in semiconductor technology development for 30 years. He is leading several emerging technology initiatives in Intel. He stated that semiconductor technology is progressing at a rapid pace. Intel has decided to expand its manufacturing capability significantly by investing about 120 B$ in coming years in bleeding edge technologies. He emphasized that Intel is keen to invest into future technologies in the semiconductor roadmap in next 1 decade and beyond. He highlighted that he/Intel has also given similar advice to European policy makers. 2D Materials based technologies are going to be a quantum jump, like what Industry did with FinFETs/3D FETs and high-k gate stack technologies in Si CMOS. It has now become part of a global act, which requires massive investment and engagement, to enable this technology for eventual volume production. It is essential to start now to develop this technology, prove in 5-7 years that India has critical mass, knowledge/IP/knowhow base in this area, for leading industries to take over tomorrow and start manufacturing in India. We have seen the same model/approach working in other bleeding edge technologies recently. Beyond Silicon, the most promising technology candidate are 2D materials. If a leading industry has to invest in this area, in a country, they will first see whether the country has invested in that technology or not. Its already happening across the globe. Hence, it is imperative for India to invest now to be future ready.

Prof. Mayank Shrivastava subsequently gave a presentation (4:15 PM to 5:00 PM)

Post presentation, inputs, and comments of distinguished members from the strategic sectors and different ministries

Dr. Sangeeta Semwal (**MietY**) appreciated the proposal and wonderful insights from the presentation. She suggested that this initiative should be taken up while keeping in mind learnings from NNetRA and INUP models. She further suggested to follow what the majority stakeholders in this meeting suggest.

Prof. Shrivastava appreciated MeitY's role in establishing several CENs across the country. He highlighted that the proposed innovation/technology hub (i.e. 2D CoE) will be engaging with several 2D technology experts in India. These experts, if they have expressed interest in solving a particular technology or engineering problem, at different places having CEN facilities, would use their local facilities to develop an engineering solution to the problem. The solution would be at the lab scale as they would be using facilities which are used by 100s of other users for several dozens of research threads. However, their solution will be used by the proposed center in terms of technology development, integration and scaling-up. One can see this center equivalent to a Semiconductor Industry or R&D Fab (say IMEC) where the industry outsources certain problems to be addressed, which require deeper investigations and research, to other academic groups. The problems outsourced will be a small fraction of overall technology development effort that the center would put in place and would be of low TRL nature (TRL 1-3). However, the proposed centre's effort will be on high TRLs (TRL 4-8). A similar model is also followed by IMEC (and also by many R&D Fabs in USA). Such deeper investigation will be pursued by 2D technology/device experts across the country, including those in IISc, using their respective institute's central facilities earlier funded by MeitY/DST/DRDO/MHRD. Once a solution is developed, the IPs, knowhow, process, etc will be transferred to the center (or the industry) under a certain pre-agreement for IP transfer. This will be the job of the 2D Research Consortium, which will be part of the proposed 2D Technology/Innovation Hub. Besides, the center would also cater to various needs to academic/scientific community in India like availability of high-quality material, availability of devices to test/investigate/experiment, availability of PDK for circuit design, availability of process knowhow, access to industries, etc. So, experts from different academia will engage with the CoE in a very similar way as anyone engages through-out the world with IMEC's center (which is only at one place in the world). IMEC focuses on a range of technologies while this center will work only on technologies based on 2D materials.

Dr. Sandip Chatterjee (MietY) disclosed a Graphene application centre being recently approved by MeitY to C-MET with the participation of TATA Steel. They are being mentored by Prof. R. R. Nair of Manchester Institute who works on graphene based membranes and coatings. This center, rather than focusing on research, will be using the existing outcome of C-MET and another university in Thrissur to convert that into technology with a focus to support local industries. More details are yet to evolve as the center was funded only recently.

Prof. Shrivastava appreciated MeitY's effort in pushing graphene's applications in various sectors. He further assured that since the proposed effort is not on Graphene's use in the technologies that C-MET is focusing on, an overlap with C-MET's center is averted naturally. The focus of the proposed innovation center/hub is on 2D Semiconductors such as Transition Metal Dichalcogenides, i.e., technologies which leading semiconductor industries (such as Intel, TSMC, etc.) are pushing and technologies which are in IRDS and Quantum roadmap. If we use graphene in our technology roadmap, it would be only because we may need to integrate Graphene with 2D Semiconductors in complex device/process integrations. He also highlighted that the proposed effort is primarily on technology development & scale-up. The proposed technology roadmap also focuses on technology development & scale-up while catering to applications like electronics, sensing, neuromorphic, optoelectronics and quantum. He further requested to share more details once available.

Dr. Murali Mohan (DST) stated that this was a very nice presentation, and it was a great learning listening to this. He further shared the following: (1) In DST there are two dedicated missions namely NMI-CPS and NM-QTA. The NM-QTA (Quantum mission) is in approval stage wherein there is one Technology hub on quantum materials & devices. Your proposed center should also bring a convergence with these initiatives. In NMI-CPS, there are 25 hubs, all section 8 companies. The proposed center may use learnings of hubs created under NMI-CPS like those in IITR, IITM and IISER-Pune, which are focusing on sensors and actuators for Cyber Physical Systems (CPS). Let's ensure there is a greater convergence across various efforts in the country if there is an overlap or if there is something for your center to learn. (2) Typical Centre of Excellence (CoE) in academic institutes, having purely academic priorities, appears to be inward looking, i.e., primarily to cater to researchers within institute to do research and publish papers. The structuring of CoE, status, activities must be well defined. Overall, CoE requires more flexibility. IP management, revenue sharing, industry co-partnering etc. are few of the areas to be addressed carefully. He suggested convergence of on-going and futuristic activities to be accounted in the DPR.

Prof. Shrivastava thanked Dr. Mohan for sharing all the details and useful guidance. He assured that the focus or purpose of CoE or innovation hub is not inward looking. The proposed CoE or innovation/technology hub will not be an academic department/center of IISc. The focus is on technology development and scale-up, which eventually is directly useful for semiconductor industries. It will be eventually a section-8 company in terms of its operation or a similar model to ensure the center has operational flexibility. SID is helping to formulate this and help developing model/policy for financial independence as well as operations just like any other industry. He also expressed gratitude to DST for useful inputs on a need to build a synergy. He assured that while the ongoing effort has already helped building a synergy with various 2D experts in India and with those who would like to get into this area, in terms of operations, execution model and technical roadmap we are committed to build synergy with some of the initiatives listed by Dr. Mohan. At the technical front, some of the experts at different places will engage directly with the center.

Dr. Sona Das (**SCL, DOS Representative)**: It was a very nice presentation and a much-needed proposal covering the electronics, sensing, neuromorphic, optoelectronic and quantum applications of 2D materials. This is an excellent initiative. Would this Centre be focusing on other 2D materials also over and above graphene, like transition metal chalcogenides, etc.?

Prof. Shrivastava answered that the focus of the proposed innovation center/hub is on 2D Semiconductors such as Transition Metal Dichalcogenides, i.e., technologies which leading semiconductor industries (such as Intel, TSMC, etc.) are pushing and technologies which are in IRDS and Quantum roadmap. If we use graphene in our technology roadmap, it would be only because we may need to integrate Graphene with 2D Semiconductors in complex device/process integrations or use Graphene for a very specific technology development, particularly of interest to industry and strategic, for example, graphene-based THz detectors, EMI shield and heat spreaders, which are not in C-MET's roadmap.

Dr. Anil Raj Singh (DRDO HQ, DRDO's Representative): Thank you for this nice proposal and presentation. Certainly, the 2D material-based technology platform is going to be the future of semiconductor technologies and replace Silicon soon. It will also help further miniaturization of electronics and other applications. He suggested that from DRDO point of view we would be looking into technology with a focus on its applications. Your technology roadmap should have timely demonstrations of technologies to keep the enthusiasm maintained throughout the duration. Besides, he asked whether the infrastructure will be located at one centre or distributed across various locations. If its at one location, how people at different locations are going to engage.

Prof. Shrivastava answered that the proposal is to have a national center, to be established as a technology/innovation hub in IISc with centralized facilities and focused effort. The infrastructure must be at one location. Semiconductor technology/product development involves integration of complex processes, all developed using a dedicated tool line inside a highly controlled environment (cleanroom). If I have to build a product which integrates 100s of processes together and 1000s of devices together, you can't develop them separately using different facilities at different locations/institutes. A fab which must be doing technology development and scale-up can't be at scattered location, therefore.

<u>How other will engage:</u> One can see this center equivalent to a Semiconductor Industry or R&D Fab (say IMEC) where the industry (or R&D Fab) outsources certain problems to be addressed, which require deeper investigations and research, to other academic groups. The problems outsourced will be a small fraction of overall technology development effort that the center would put in place and would be of low TRL nature (TRL 1-3). However, the proposed centre's effort will be on high TRLs (TRL 4-8). A similar model is also followed by IMEC in Europe (and by many R&D Fabs in USA). Such deeper investigation will be pursued by 2D technology/device experts across the country, including those in IISc, using their respective institute's central facilities earlier funded by MeitY/DST/DRDO/MHRD. Once a solution is developed, the IPs, knowhow, process, etc will be transferred to the center (or the

industry) under a certain pre-agreement for IP transfer. This will be the job of the 2D Research Consortium, which will be part of the proposed 2D Technology/Innovation Hub. This way the proposed national centre or innovation hub in IISc will also cater to everyone's need in India and truly engage with every contributor in the country, just like IMEC, etc. Besides, the center would also cater to various needs to academic/scientific community in India like availability of high quality material, availability of devices to test/investigate/experiment, availability of PDK for circuit design, availability of process knowhow, access to industries, etc. So, experts from different academia will engage with us in a very similar way as anyone engages through-out the world with IMEC's center (which is only at one place in the world). IMEC focuses on a range of technologies while this center will work only on technologies based on 2D materials. This center or innovation hub will also call for transfer of technology, which might have already been developed in specific groups.

This kind of scale-up is not the charter of individual research groups. This must happen inside a dedicated process line. Only after integration and scale-up of the technologies, which must be done at a central location, using a dedicated (professionally run) Fab line, investors and industry will pitch-in. Industries are not interested in small modules or publications, they want full-fledged products. We must also understand that everyone involved in development doesn't need to be co-located at the center. This is how industry works. Except the engineers who are running the tools/process and the PI team involved in process development and operations, everyone else would work/contribute remotely. Then physical location can be anything. We need to understand that the kind of facility we will be developing will not be like other multi-user facilities in the country. It will be operated by dedicated trained professionals, and not by students and research staff of individual groups. This is how R&D Fabs work. He further requested Dr. Harald Gossner to add to this.

Prof. Harald Gossner, in response to the request above, highlighted that TMD based technologies are major endeavour now for semiconductor industry. This is not basic research anymore. This requires dedicated effort and involves developments including various integration stages and integration of various process modules into a final flow. This center should focus on everything involved before high volume development – say everything at an early scale-up and development phase. This center should take the technology to a point from where Industry can take it further for high volume manufacturing. Once that is done Industry like Intel would be investing Billions. But this requires sophisticated integration using one dedicated Fab line. This can't happen in scattered fashion. But having said that, the people involved in development can be located at different locations, they don't need to be present where manufacturing happens. They can be present at different places. If you see IMEC model, in the initial days (many decades back), they had scattered facilities. Soon they realized that you can't do anything by having scattered facilities. Then they integrated at one place, became useful for industry, while still catering to universities around or engaging with universities around. I hope this answers the question.

Dr. Anil Raj Singh thanked Dr. Gossner. He asked whether some parallel development will also be taken-up while IISc will be setting-up the center / innovation hub.

Prof. Shrivastava explained that the plan is, while we will be building the Fab line, which will take initial 2 years, the center will fund specific developments to 2D technology experts in India (experts across institutes, including IISc) through a competitive call. The thrust area and scope of work will be derived out of the proposed technology roadmap of this proposal. The scope of work will be extremely detailed, with clear development goals while ensuring that the developed module can eventually be integrated in the universal process or technology platform that we would be developing in the proposed center. So, in some sense, it will be a joint/collaborative effort. Those who take-up certain module developments will transfer the process/module to this center by the end of 2 years (through a pre-agreed IP transfer agreement) and in subsequent years. The call will follow the international SRC (Semiconductor Research Consortium) model, which is being executed successfully by the international semiconductor industry consortium since few decades. The proposals and projects will be reviewed by an international advisory / review board.

Dr. Anil Raj Singh thanked Prof. Shrivastava and IISc team and expressed DRDO's wholehearted support for this endeavour.

Prof. Tarun Sharma (RRCAT, DAE): He congratulated for a wonderful presentation and an ambitious vision for the country as well as proposal to build a world class center. He appreciated the clear roadmap while emphasizing that a lot of things can be done in this area and must be done in the country. He highlighted that sooner we start, it will be better for the nation. He further stated that there are several new developments in quantum technology using 2D materials. We must see how it can be connected to national mission on quantum technology because of common interests. He emphasized that for the budget and vision proposed, it must be a single center rather than having scattered activities or multiple such centers. The center must be accessible across the nation through the modes presented in this presentation. Certainly, we must have world class facility and it shouldn't be limited by any limit being set on the funds. Without great facility and infrastructure, the kind of goals this center envisions can't be fulfilled. From DAE and RRCAT point of view, we have been working on various aspects of 2D materials for example applications in light sources, Spin photonics and valleytronics, Qubits, etc. If this center comes and provide us electronic grade 2D materials on large area wafers and later the process, that will be a great push for several developments of strategic nature like optoelectronics, quantum, and sensing. Sensors for pressure, temperature and radiation sensing requires ultra-high sensitivity and ultra-fast speed and robustness. Besides, there are several other strategic applications too. He stated that he looks forward to this initiative as this a wonderful initiative and it must be taken-up soon.

Questions & Discussions with Academic Peers:

Prof. Ahuja (Director, IIT Ropar): He appreciated the work and presentation. He disclosed that he was part of the graphene flagship program in Sweden before he

moved to India recently. He emphasized that though we are late in this initiative, we must not delay any further. This initiative should be taken-up immediately. He suggested that we should not follow Graphene flagship model which was highly scattered across the entire Europe with 200 universities involved. He highlighted that when things are scattered, nothing concrete comes out. He emphasized that this must be a focused effort with a single center as proposed in this presentation. This effort should focus more on 2D materials and less on graphene. He gave examples of Manchester and Cambridge centers which have focused efforts. He stated that India has the critical mass, what is now required is to have a focused effort in some key areas related to 2D materials, examples electronics, sensing, memory, neuromorphic and up to a certain extent a few areas in Quantum. And, if we do this, we will be able to make a noticeable dent in the area of 2D material's based emerging applications.

Prof. Shrivastava thanked Prof. Ahuja for useful insights while highlighting that the emphasis is on 2D materials and a focused effort as he suggested.

Prof. H.K. Singh (NPL): He suggested to not miss metrology requirements when the focus is on developing technology. He extended NPL's support in calibrating all characterization and metrology equipment.

Prof. Shrivastava thanked him for the support.

Prof. V.C. Srivastava (IIT Roorkee) suggested to also have a roadmap on other 2D materials in bulk form such as graphene oxide, etc. to be produced in India as such materials, which may not be in large area monolayer forms, are also required in applications such as printed electronics, automobiles, etc. This center should enable such developments within the country and connect people - who are developing - with people who require such materials.

Prof. Shrivastava explained that the center will develop electronic grade large area materials grown using MOCVD, MBE etc. Growth of such bulk 2D materials will not be in the charter of the proposed center. The center, however, can enable, as suggested by Prof. V. C. Srivastava, development of bulk 2D materials across different institutes in India and local industries and then connect them with people/groups/organizations/ministries which require such materials. This activity is much easier as it doesn't require the kind of infrastructure required in developing electronic grade materials, and thus can be undertaken at different institutes. However, the center will keep itself excused from anything related to application of bulk 2D materials.

Prof. Marshal (IIT BHU): He asked the following while emphasizing that he is looking forward to this center and he would like to extend all possible support:

- While the facility will take 2 years to come up, how we would be able to participate during this initial phase and what will be our role?
- Is it a pre-requisite to have a proof-of-concept for device scalability or at what level can people participate?

- What kind of logistic support/fund will be provided if a user from industry/academia wants to use the facility?

Prof. Shrivastava explained that the development of technologies such as electronics, sensing, neuromorphic, optoelectronics or quantum, happens in a modular fashion. Initially various process and unit step modules will be developed such as large area growth, contacts, gate stacks, transfer, heterostructures, patterning, passivation, back-end-of-the-line, etc. Then these modules will be integrated, and process will be fine-tuned before scaling-up can be done. During the scale-up you also investigate other aspects such as yield, reliability, and variability. Hence, several threads require iterations at various level – from material growth till full product. However, some of the thread which do not require iteration or physical presence at the center, can be taken up by experts around the country. These could be, for example solving an engineering problem related to process or development efforts such as PDK, reliability qualification, modeling etc.

Besides, there are several low TRL threads, like optoelectronics and quantum, which are also going to be supported in the initial years. This will be further scaled-up at this center. This will also be taken-up by various experts through competitive call.

Those who wish to scale-up their ideas, proof of concept is a must before it can be transferred to this center. This center is not for doing basic research or exploratory studies. For explorations, MeitY has already established CEN facilities across the country. This center is for technology development and scale-up. As a biproduct of the in-house developments, this center will cater to needs to academic community for their scientific explorations (such as availability of material, devices, PDK, testchip, MPW shuttles, etc).

One can see this center equivalent to a Semiconductor Industry or R&D Fab (say IMEC) where the industry outsources certain problems to be addressed, which require deeper investigations and research, to other academic groups. The problems outsourced will be a fraction of overall technology development effort that the center would put in place and would be of low TRL nature (TRL 1-3). However, the proposed centre's effort will be on high TRLs (TRL 4-8). A similar model is also followed by IMEC (and also by many R&D Fabs in USA). Such deeper investigation will be pursued by 2D technology/device experts across the country, including those in IISc, using their respective institute's central facilities earlier funded by MeitY/DST/DRDO/MHRD. Once a solution is developed, the IPs, knowhow, process, etc will be transferred to the center (or the industry) under a certain pre-agreement for IP transfer. This will be the job of the 2D Research Consortium, which will be part of the proposed 2D Technology/Innovation Hub. Besides, the center would also cater to various needs to academic/scientific community in India like availability of high-quality material, availability of devices to test/investigate/experiment, availability of PDK for circuit design, availability of process knowhow, access to industries, etc. So, experts from different academia will engage with us in a very similar way as anyone engages through-out the world with IMEC's center (which is only at one place in the world). IMEC focuses on a range of technologies while this center will work only on technologies based on 2D materials.

Prof. Rajesh Kumar (IIT Indore): Thank you for involving everyone in this discussion. In such a large project, since out of the 50-100 Cr. of funding will be budgeted for research performed by groups outside this center, wouldn't it be good to identify small clusters at different institutes/university/college level, so that everyone even at the smallest level is on board and not missed out.

Prof. Shrivastava emphasized that one needs to find a sweet spot between being focused and being too scattered. On one hand, we need to have a focus and deliver technology & on other hand we must cater to the majority needs. In order to make a dent in the international 2D community through this effort, we need to find a sweet spot in a focused manner.

Prof. Pramoda Nayak (IIT Madras) appreciated the effort and suggested the following:

- While for large scale application and technology scale-up, as you proposed, you need large area growth of materials using industry standard tools in a professional environment. However, few of us explore or development these materials at lab scale (say few micro-meters to millimetre level). Can your center connect people who can develop lab scale material with groups who are need of such material for their lab level explorations?
- Take advantage of expertise available in India, at different places.
- In addition to one big centre at IISc, which must happen, would there be possibility of small clusters at 3-4 different locations in India, to put efforts on lab scale explorations. The outcome of these clusters can then be transferred to the center proposed for scale-up.

Prof. Shrivastava appreciated the suggestions. He emphasized that of the objective of this center will be to connect different experts in different area across the country and Indian diaspora. The center will also take advantage of expertise and technology knowhow/IP available across the country. This has already been requested through the google form. And if there are lot of IPs indicated in the form and then dedicated efforts will be budgeted in the DPR to licence these IPs in the center for further scale-up. Moreover, we can add in the DPR that the government should explore ways to have few more clusters beyond this CoE, in the subsequent phases, that will also enable further growth of the centre in future. The Google form is made to capture all the available details w.r.t development, technology licensing, expertise, etc. that will help to bring everyone in the country on board to participate in this dedicated effort to scale -up the industry-oriented useful technology. The individual cluster location would be a function of groups contributing to technology development / explorations / transfer in phase I.

Mr. Manish Anand (Incubator at IIT Roorkee): What is the kind of interest that the industry has shown in this project? Have you identified any industry partner who is ready to invest in the beginning itself? At IITR Incubator we have suggested local industries to invest 10% cash to pressure test on their requirements.

Prof. Shrivastava: Semiconductor is not a "local industry" business. It's a global business which requires 100s of B$ investment. India doesn't have this luxury yet.

However, our hope is that this center will generate enough traction to attract leading industries to invest in India. Hence the focus in the beginning must be to attract leading multinational industries. Later, through spin-off of this center local industries and start-ups will be created. The potential industries which have expressed interest in this CoE are Intels of the world. These are mostly semiconductor giants, multinational companies and investors who are investing in deep-tech start-ups worldwide. Their funding models are different to local Indian industries. Such companies pitch to fund only when buy-in from govt. is in place and the center/facilities are in a certain shape (govt. buy-in is a must, but not always enough for these companies to invest – a reason why we still don't have a Fab from any of these leading players despite their strong presence in design sector). In context of 2D technologies, these companies have access to other centers (like IMEC) and therefore for them there is no reason to invest without having the plan approved by the govt. They are not under any pressure that we can test by asking to pay upfront cash. We, as a country, are under pressure to not miss another bus. The best way these industries can show interest at this stage is by a written expression of interest (even that goes through a lot of vetting by their legal and senior management). Similarly, investors funding deep-tech initiatives don't pitch-in at this initial stage. They will pitch-in only if the technology has crossed TRL 5 or 6. We are in talks with them to learn at what stage they would pitch in and how do we strategize our roadmap to have them on board as early as possible. The bottom line is that this center is India's pressing need. This center must enable a local industry base for deep-tech emerging technologies, which doesn't exist yet. History tells such industries are incubated out of such efforts / technology hubs, not the other way around. So, if we wait for an industry to fund such an effort, it's never going to happen, and India will miss another bus.

Prof. Bipin Kumar (NPL): This was an excellent initiative with nice idea and a great dream. Please ensure the following three, (1) State-of-the-art development, investment, and facilities, (2) systematic plan leading to (3) industry relevant high yield technologies. It should not be like an academic setup and to publish papers. State-of-the-art centre and development can also help generating earning, for example if you produce high quality material, devices, platform for developing circuits, etc., there are 100s of institutes in India which will be interested in utilizing that, besides industries pitching in to utilize the outcome.

Prof. Shrivastava: You have very rightly said. The scale and quality with a dedicated state-of-the-art process line is very important for such a development. In academic set-up/lab, the yield of the material and devices is limited, which hinders product development. For systems, which involve integration of large number of devices over a given material, one needs high material yield, high yield of devices and circuits, for successful integration. In the roadmap of this CoE, we will be engaging with leading industries in material growth. There is a written commitment from tool companies by which they will invest in terms of tools, people, and process in this centre in trade of material knowledge and its behaviour in devices and system. Thus, the material, it's scale, quality and reliability are going to addressed right from the beginning of the project. Dedicated process line will high yield, high quality, and

high reliability devices. These in turn will result in high yield circuits and systems. In the quantum domain, the quality of material and devices is very critical. Hence, focus will always be on quality, yield, scale, reliability, variability so that other emerging areas can also be catered through the universal technology platform that we develop. On your second point, yes, the idea is to grow large area, high quality 2D materials by MOCVD or MBE, in large quantity, that can be employed to the country's needs as well as be useful in technological developments projected herein.

Dr. Kaushik Ghosh (INST Mohali): We have developed carbon-based matrix at CMOS compatible temperature with a Focus on developing high quality, high crystallinity material.

Prof. Piyush Chaubey: This is excellent initiative. As this initiative is technology driven, which is how it should be, there is lots of scope for experimental work. However, is there any role for theoretical and computational research in 2D materials, in particular, for those bordering more on the fundamental aspects which may find technological applications after around 10 years?

Prof. Shrivastava: Yes, we have a 10+ year vision. The 2D CoE effort will also cater to fundamental aspects under the following two threads i.e., computational, and experimental, if they are technologically relevant a few years down the line. These are the low TRL threads that we will pursue from the beginning along with high TRL activities.

Prof. Govind (NPL): Thank you. First, this is an excellent initiative. I agree various aspects need to be addressed for developing industrially relevant technologies. I am curious, What will be the role of growers or material scientists in India if the material growth recipes are taken from tool companies?

Prof. Shrivastava: From material growth point of view, CoE will be interested to collaborate with groups having high quality electronic grade material growth technology, well demonstrated over large areas (say a few inch and beyond). If there are Indian growers, who can licence a material growth technology as good as what the leading players have, CoE proposes to licence that too. The Google form shared with everyone is an attempt to capture all the details (technology transfer or licensing) from industry as well as Indian researchers. The end goal is scalable technology showing heterogenous integration which is of technological and industrial importance. The same is true from device technology front, i.e., CoE is open to license device technologies or established process flows. If they are not there, we are proposing separate funds to fund such developments, which eventually can be transferred to CoE. This entire development will produce enough problem statements that everyone's needs can be met. For example, for a grower, how to grow defect free heterostructures, how to engineer material for transistor applications and memory applications independently, as their requirements are different, etc. What we will get from the material growth tool companies will be a base process. When we run that material through a certain device process, we will experience several material specific challenges. These challenges will be shared with material growers in India to solve. Besides, Indian growers will also have an opportunity to test their materials through a qualified device process using device level figure of

merit parameters. This kind of experience is hard to get for any material grower (at the end of the day, your material must give desired device characteristics – just material specific parameters don't qualify whether a material is good for device level application where high yield and reliability becomes extremely critical). So, in a nut shell, there will be a lot of new and exciting opportunities for material growers when they collaborate with the CoE and device community.

Dr. Seena V: This was an excellent presentation with a great vision for the country. Many of us have struggled with 2D materials and therefore we can see the value of this center. I would like to know what kind of contribution Industry will offer, especially for 2D material growth and unit process development?

Prof. Shrivastava: The industry has promised to offer their high-end industry standard growth tools, growth recipe, and support personnel to deliver high quality electronic grade material which they already have through their developments at other places like IMEC, Cambridge, 2D-EPL, etc. They have promised to transfer all this in return of learning how their material behaves when you run the entire device/circuit process and what challenges/issues that might require further material engineering. This will help us co-design material, device and process together with the goal of achieving desired performance with high yield and reliability. For the unit process development, we will be completely independent of industry, but will develop something that would be of use by them.

Dr. Seena V: During this material development phase, whether the material will be available to other researchers, from the initial phase? Materials of different grades are used for different applications and all applications may not require (like MEMs and Sensors) the same quality as required for transistors and optoelectronic devices. So, if material is available from the beginning, it will help researchers to give feedback and contribute in whatever way possible.

Prof. Shrivastava: Yes, it will be available from the beginning and the center will be open to get all kind of feedback.

Dr. Seena V: Is this centre going to have entire unit process development aspects covered specifically for 2D materials and then integrate into the proposed process line?

Prof. Shrivastava: Yes. Unit process and integration goes hand-in-hand. Even if certain modules are developed elsewhere, we will only use the transferred learnings from other places. They must be re-calibrated, re-develop and fine-tuned here within the constraints of process tools that we install under 2D CoE. We have also developed the entire process here in IISc, but when we transfer it to a dedicated line, it will be required to be re-calibrated, re-develop and fine-tuned. This also justifies the requirement of a dedicated line that enables integration of the modules.

Dr. Seena V: Yes, one can't process different modules at different places and integrate without any effort. Development at individual facility/university cleanrooms and then integrating them in a main fab is unrealistic. It doesn't work. I agree that you must have a dedicated process line.

Dr. Seena V: I would suggest having some flexibility in the R&D effort so that it's a two-way exchange.

Prof. Shrivastava: Thanks for iterating that. As you rightly pointed out, technology development doesn't happen in a scattered way. On the R&D flexibility, we certainly have this in our vision and proposed execution model to ensure we get inputs from all possible stakeholders and we also cater to everyone possible in the country.

Dr. Mukesh Kumar: Thank you for this nice presentation and initiative. Most of my questions are already addressed through previous questions. My last question is, is it true that this proposed center or innovation hub for developing industry relevant technologies and their scale-up?

Prof. Shrivastava: Yes, the objective is to develop Electronics, Sensing, Neuromorphic, Memory, Optoelectronics & Quantum technologies, relevant to industries – as suggested by industry roadmap – to different TRLs.

Dr. Mukesh Kumar: Thanks. So, my follow-up question is how do you plan to utilize the expertise from different institutions? For example, if I have expertise in photodetectors, how would I be able to contribute.

Prof. Shrivastava: Think of this center like an industry or an innovation hub. We will engage with experts across the country through a competitive call (like SRC model) based on thrust areas derived out of the technology roadmap of the proposed center. The outcome of these developments elsewhere will be integrated into our developments. The second way is by transferred technology to this center. We have requested everyone to capture this aspect through the Google form shared, if anyone has a specific technology, which one wants to transfer or license to the CoE. The technology transfer should be within the technology roadmap and should also be scalable. There are few other modes, as I have explained in response to earlier questions (like the one answered in response to questions specific to material growers and people working on 2D MEMs, Sensors and Quantum devices).

Prof. Balakrishnan: Thank you, I really enjoyed this presentation and I really appreciate this focused initiative. I have also gone through your roadmap paper and the proposal. To compensate for the 10 years of loss, you are starting this initiative at the right time. I agree with most of the discussions. I have one point to highlight. In an initiative of this kind, with effort on indigenous technology development, we shouldn't rely on to imported material and growth tools. Although this is done to cover up the time lag, some effort in large scale manufacturing specially CVD growth and scale-up of the electronic grade materials under the same center. Also, sharing of the benchmark and other qualifying parameters with other growers in India will help these researchers to align their research with the requirements of this center and industry.

Prof. Shrivastava: Thank you, these are extremely valid point. The idea of the CoE is not to diminish "Make in India" effort. The tool companies have offered only the process/recipe and experience to scale it up here locally. We will not be relying on imported materials, but only on a base recipe to get a head start. The quality of material will be improved locally through the feedback from the process. Besides, as

you rightly pointed out, benchmarks and inputs will be shared with the growth community to align their research with the requirements of industry.

Prof. Balakrishnan: Thank you, I am looking forward to this innovation hub / 2D center in India.

Mukesh Kumar (IIT Indore): This is an excellent effort at the right time. Thanks for envisioning this center and putting effort on this CoE. I believe this is also aligned with India semiconductor mission. Some applications may require co-integration of CMOS based circuits with 2D based technology to integrate outcome of your center with the upcoming Si Fab in India.

Prof. Mayank: Thank you, this is a very valid point. In fact, what IMEC and industry is doing current is precisely the same. They are building 2D process on their 300mm line to eventually integrate 2D circuits with CMOS circuits, possibly in CMOS backend. The reason they started with 300mm line because they wanted to co-integrate with the CMOS process which they run in 300mm wafer line. Therefore, I highlighted in my presentation that the augmentation of Si CMOS with 2D circuits will happen much before dedicated 2D based products. So, thanks for this input and we will keep this aspect in our technology development roadmap to enable integration with the Si CMOS flow as well.

Prof. Sharma (RRCAT, DAE) I would like to add to your answer in response to question from Dr. Govind of NPL and Prof. Balakrishnan. Growers shouldn't feel that if this center comes with industry grade growth tools with growth recipes, then they will not have much to contribute. I, in fact, think that the growers and similarly device engineers in India will be able to push their research to the next level if this center comes. While growers will have opportunity to solve industrially relevant problems, they will also have a taker. Besides, they will get benchmarks and device level feedback from this center. For the scale of technologies, and given the complexities in developing semiconductor process, the full process should be available at the centre which demands a dedicated process line. Scattered efforts don't work when you develop technology which requires extremely complex integration and have tight process margins. But if this comes, researchers/scientists across the country will need less time to realize their idea as they will not be required to re-invent the wheel such as growth, contacts, process optimization, etc. The CoE model urges aiming for industry-driven devices and technologies. Once these are achieved, it will generate enough traction that leading industries will pitch in and take it forward. Besides, it will also give birth to several spin-off in the country. Unless you don't create a world class facility, you won't be able to make a dent.

Prof. Balakrishnan and Dr. Govind thanked Prof. Sharma for clarifications and highlighted that this is what they also wanted to emphasize.

Prof. Shrivastava thanked everyone for wonderful inputs and questions. He stated that these 3 hours were spent quite well. He expressed hope that he would have answered everyone questions. He further requested everyone to fill the shared google form if there are any more input. He requested everyone's strong support and blessings for this ambitious endeavour. He emphasized that we need to be ambitious

to make a dent as other eminent members also stated. He subsequently requested PSA's office to conclude.

Mr. Sirish Panda (PSA's Office): This was an extremely productive meeting. The number of valuable inputs and the discussion was beyond expectations. I think there is an excellent roadmap to begin with. I would like to congratulate IISc Bangalore to take-up this excellent and timely initiative. PSA office will offer all support and help to develop this DPR and to connect with any other stakeholder, industry or govt body.

*****